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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/045,354	11/07/2001	Angela Hui	AF01159	1692
29393	7590	02/24/2004	EXAMINER	
ESCHWEILER & ASSOCIATES, LLC NATIONAL CITY BANK BUILDING 629 EUCLID AVE., SUITE 1210 CLEVELAND, OH 44114			NGUYEN, KHIEM D	
			ART UNIT	PAPER NUMBER
			2823	

DATE MAILED: 02/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/045,354

Applicant(s)

HUI ET AL.

Examiner

Khiem D Nguyen

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 08 December 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-24 and 27 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-24 and 27 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 07 November 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ 6) ☐ Other: _____

DETAILED ACTION

The indicated allowability of claims 19-24 and the objected claims is withdrawn in view of the newly discovered reference(s) to Cheng et al. (U.S. Patent 6,159,821) and Yu (U.S. Patent 5,998,278). Rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 1-5, and 7 are rejected under 35 U.S.C. 102(e) as being anticipated by Cheng et al. (U.S. Patent 6,159,821).

In re claim 1, Cheng discloses a method of stripping a hard mask from a substrate comprising an insulating material (FIG. 2: 12) (col. 2, lines 34-36) exposed within gaps (FIG. 2: 16) (col. 2, lines 33-44) patterned through the hard mask (FIG. 2: 14), comprising (col. 2, line 33 to col. 3, line 51 and FIGS. 1-11): coating the substrate (FIG. 2: 10) with a sacrificial material (FIGS. 3-4: 17) that fills the gaps (col. 2, lines 45-48); and plasma etching (col. 2, lines 54-64) to strip the sacrificial material and the hard mask “substantially” completely in a single plasma etch process (FIGS. 4-5).

In re claim 2, Cheng discloses wherein the hard mask material comprises a nitride (col. 2, lines 36-38).

In re claim 3, Cheng discloses wherein the hard mask material comprises SiN (col. 2, lines 36-38).

In re claim 4, Cheng discloses wherein the insulating material comprises an oxide (col. 2, lines 34-36).

In re claim 5, Cheng discloses wherein the insulating material comprises a material selected from the group consisting of silicon oxide (col. 2, lines 34-36).

In re claim 7, Cheng discloses wherein the plasma etching is carried out with gases comprising a fluorinated hydrocarbon (CHF_3) and oxygen (col. 2, lines 54-64).

2. Claims 10 and 13-15 are rejected under 35 U.S.C. 102(e) as being anticipated by Cheng et al. (U.S. Patent 6,159,821).

In re claim 10, Cheng discloses a method of stripping a hard mask from a substrate comprising an insulating material (FIG. 2: 12) (col. 2, lines 34-36) exposed within gaps (FIG. 2: 16) (col. 2, lines 33-44) patterned through the hard mask (FIG. 2: 14), comprising (col. 2, line 33 to col. 3, line 51 and FIGS. 1-11): coating the substrate (FIG. 2: 10) with a sacrificial material (FIGS. 3-4: 17) that fills the gaps (col. 2, lines 45-48); and plasma etching (col. 2, lines 54-64) to strip the sacrificial material and the hard mask “substantially” completely in a single plasma etch process (FIGS. 4-5); wherein the hard mask is employed to etch a layer or bulk portion of the substrate comprising silicon (col. 2, lines 36-44 and FIGS. 1-2).

In re claim 13, Cheng discloses wherein the hard mask material comprises a nitride (col. 2, lines 36-38).

In re claim 14, Cheng discloses wherein the hard mask material comprises SiN (col. 2, lines 36-38).

In re claim 15, Cheng discloses wherein the insulating material comprises an oxide (col. 2, lines 34-36).

3. Claims 11, 19 and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Cheng et al. (U.S. Patent 6,159,821).

In re claim 19, Cheng discloses a method of stripping a hard mask from a silicon containing surface, comprising (col. 2, line 33 to col. 3, line 51 and FIGS. 1-11): providing a sacrificial material (FIGS. 3-4: 17) that covers the hard mask and fills gaps (FIG. 2: 16) in the surface patterned with the hard mask (col. 2, lines 33-48); and plasma etching (col. 2, lines 54-64) to remove “substantially” completely the hard mask and that portion of the sacrificial material that covers the hard mask in a single plasma etch process (FIGS. 4-5).

In re claim 11, Cheng discloses wherein the hard mask is employed to etch a silicon wafer (col. 2, lines 33-44 and FIGS. 1-2).

In re claim 20, the sacrificial material as discloses by Cheng would inherently serve to protect an oxide within the gaps through at least a portion of the plasma etching. Note that the disclose process would obtain the recited results because the same materials are treated in the same manner as in the instant invention.

4. Claim 27 is rejected under 35 U.S.C. 102(e) as being anticipated by Cheng et al. (U.S. Patent 6,159,821).

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In re claim 27, Cheng discloses a method of stripping a hard mask from a substrate comprising an insulating material (FIG. 2: 12) (col. 2, lines 34-36) exposed within gaps (FIG. 2: 16) (col. 2, lines 33-44) patterned through the hard mask (FIG. 2: 14), comprising (col. 2, line 33 to col. 3, line 51 and FIGS. 1-11): coating the substrate (FIG. 2: 10) with a sacrificial material (FIGS. 3-4: 17) that fills the gaps (col. 2, lines 45-48); and plasma etching (col. 2, lines 54-64) to strip the sacrificial material and the hard mask in a single plasma etch process (FIGS. 4-5).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 6, 8, 9, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cheng et al. (U.S. Patent 6,159,821) as applied to claims 11, 19 and 20 above, and further in view of Hemmenway et al. (U.S. Patent 5,270,265) and Yu (U.S. Patent 5,998,278).

In re claim 6, Cheng does not explicitly disclose wherein the sacrificial material comprises a material selected from the group consisting of resists and organic BARC materials.

Hemmenway discloses a method of stripping a hard mask from a silicon containing surface, comprising: providing a sacrificial material (FIG. 4: 51) that covers the hard mask (FIG. 4: 11) and fills gaps (FIG. 4: 43) in the surface patterned with the hard mask wherein the sacrificial material comprises a material selected from the group

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consisting of resists (col. 4, lines 32-45); and plasma etching to remove “substantially” completely the hard mask and that portion of the sacrificial material that covers the hard mask (col. 3, line 46 to col. 4, line 26 and FIGS. 4-8). It would have been obvious to one of ordinary skill in the art of making semiconductor devices to combine the teaching of Cheng and Hemmenway to enable the sacrificial material of Cheng to be formed and furthermore to protect the bottom of the trench pattern during etching of the hard mask oxide (col. 2, lines 8-19).

In re claim 8, Hemmenway discloses wherein plasma etching completely removes the sacrificial material from the gaps (col. 3, line 61 to col. 4, line 4 and FIG. 8).

In re claim 9, the process of spin-coated a sacrificial material onto the substrate is well-known to one of ordinary skill in the art of making semiconductor devices.

In re claim 12, Yu discloses wherein the hard mask (FIG. 2B: 23a) is employed to etch an polysilicon (FIG. 2A: 22a) (col. 2, lines 55-65). It would have been obvious to one of ordinary skill in the art of making semiconductor devices to combine the teaching of Cheng and Yu so that a shallow trench isolation is accomplished (col. 2, lines 32-34).

6. Claims 16-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cheng et al. (U.S. Patent 6,159,821) as applied to claims 10 and 13-15 above, and further in view of Hemmenway et al. (U.S. Patent 5,270,265).

In re claim 16, Cheng does not explicitly disclose wherein the sacrificial material comprises a material selected from the group consisting of resists and organic BARC materials.

Hemmenway discloses a method of stripping a hard mask from a silicon containing surface, comprising: providing a sacrificial material (FIG. 4: 51) that covers the hard mask (FIG. 4: 11) and fills gaps (FIG. 4: 43) in the surface patterned with the hard mask wherein the sacrificial material comprises a material selected from the group consisting of resists (col. 4, lines 32-45); and plasma etching to remove “substantially” completely the hard mask and that portion of the sacrificial material that covers the hard mask (col. 3, line 46 to col. 4, line 26 and FIGS. 4-8). It would have been obvious to one of ordinary skill in the art of making semiconductor devices to combine the teaching of Cheng and Hemmenway to enable the sacrificial material of Cheng to be formed and furthermore to protect the bottom of the trench pattern during etching of the hard mask oxide (col. 2, lines 8-19).

In re claim 17, Hemmenway discloses wherein plasma etching completely removes the sacrificial material from the gaps (col. 3, line 61 to col. 4, line 4 and FIG. 8).

In re claim 18, the process of spin-coated a sacrificial material onto the substrate is well-known to one of ordinary skill in the art of making semiconductor devices.

7. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yu (U.S. Patent 5,998,278) in view of Cheng et al. (U.S. Patent 6,159,821).

In re claim 21, Yu discloses a method of removing a hard mask, comprising: forming an oxide region (FIG. 2B: 26) over a semiconductor substrate (FIG. 2B: 20), forming a silicon layer (FIG. 2A: 22a) over the semiconductor substrate, wherein the silicon layer covers the oxide region, forming and patterning a hard mask layer (FIG. 2B: 23a) over the silicon layer; etching a gap (FIG. 2B: 25) in the silicon layer to expose a

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portion of the oxide region using the patterned hard mask as an etch mask; forming a sacrificial layer (FIG. 2C: 27) over the semiconductor substrate, thereby covering the hard mask layer and filling the gap; removing “substantially” completely the sacrificial layer and the hard mask layer (FIGS. 2C-E) with a single dry etch (col. 3, lines 20-31), wherein an etch rate of the sacrificial layer and the hard mask layer is about the same, and wherein the etch rate of the hard mask layer is substantially greater than the silicon layer.

Alternatively, Cheng discloses plasma etching (col. 2, lines 54-64) to strip the sacrificial material and the hard mask “substantially” completely in a single plasma etch process (FIGS. 4-5). It would have been obvious to one of ordinary skill in the art of making semiconductor devices to combine the teaching of Yu and Cheng to enable the single plasma etch process of Yu to be performed and furthermore to protect the surface of the substrate from etch damage (col. 3, lines 3-10).

There is no evidence indicating the etch rate of the sacrificial and the hard mask layer and the silicon layer is critical and it has been held that it is not inventive to discover the optimum or workable etch rate of a result-effective variable within given prior art conditions by routine experimentation. See MPEP § 2144.05. Note that the specification contains no disclosure of either the critical nature of the claimed dimensions of any unexpected results arising there from. Where patentability is aid to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

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8. Claims 22 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cheng et al. (U.S. Patent 6,159,821) as applied to claim 21 above, and further in view of Hemmenway et al. (U.S. Patent 5,270,265) and Yu (U.S. Patent 5,998,278).

In re claim 22, Cheng does not explicitly disclose wherein the sacrificial material comprises a BARC layer or a photoresist layer.

Hemmenway discloses a method of stripping a hard mask from a silicon containing surface, comprising: providing a sacrificial material (FIG. 4: 51) that covers the hard mask (FIG. 4: 11) and fills gaps (FIG. 4: 43) in the surface patterned with the hard mask wherein the sacrificial material comprises a photoresist layer (col. 4, lines 32-45); and plasma etching to remove “substantially” completely the hard mask and that portion of the sacrificial material that covers the hard mask (col. 3, line 46 to col. 4, line 26 and FIGS. 4-8). It would have been obvious to one of ordinary skill in the art of making semiconductor devices to combine the teaching of Cheng and Hemmenway to enable the sacrificial material of Cheng to be formed and furthermore to protect the bottom of the trench pattern during etching of the hard mask oxide (col. 2, lines 8-19).

In re claim 23, Yu discloses wherein forming the sacrificial layer comprises baking the sacrificial layer, thereby substantially planarizing the sacrificial layer (col. 3, lines 8-18). It would have been obvious to one of ordinary skill in the art of making semiconductor devices to combine the teaching of Cheng and Yu so that a shallow trench isolation is accomplished (col. 2, lines 32-34). The process of spinning coating a sacrificial material over the semiconductor substrate is well-known to one of ordinary skill in the art of making semiconductor devices.

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9. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yu (U.S. Patent 5,998,278) in view of Cheng et al. (U.S. Patent 6,159,821).

In re claim 24, Yu discloses a method of removing a hard mask, comprising: forming an oxide region (FIG. 2B: 26) over a semiconductor substrate (FIG. 2B: 20), forming a silicon layer (FIG. 2A: 22a) over the semiconductor substrate, wherein the silicon layer covers the oxide region, forming and patterning a hard mask layer (FIG. 2B: 23a) over the silicon layer; etching a gap (FIG. 2B: 25) in the silicon layer to expose a portion of the oxide region using the patterned hard mask as an etch mask; forming a sacrificial layer (FIG. 2C: 27) having a relatively planar top surface over the semiconductor substrate, the sacrificial layer comprising a portion covering the hard mask layer and a portion filling the gap; and removing “substantially” completely the sacrificial layer and the hard mask layer (FIGS. 2C-E) with a single plasma etch process (col. 3, lines 20-31), wherein an etch rate of the sacrificial layer and an etch rate of the hard mask layer are selected to substantially completely remove the portion of the sacrificial layer covering the hard mask and the hard mask layer, and wherein the etch rate of the hard mask layer is substantially greater than the silicon layer.

Alternatively, Cheng discloses plasma etching (col. 2, lines 54-64) to strip the sacrificial material and the hard mask “substantially” completely in a single plasma etch process (FIGS. 4-5). It would have been obvious to one of ordinary skill in the art of making semiconductor devices to combine the teaching of Yu and Cheng to enable the single plasma etch process of Yu to be performed and furthermore to protect the surface of the substrate from etch damage (col. 3, lines 3-10).

There is no evidence indicating the etch rate of the sacrificial and the hard mask layer and the silicon layer is critical and it has been held that it is not inventive to discover the optimum or workable etch rate of a result-effective variable within given prior art conditions by routine experimentation. See MPEP § 2144.05.

Response to Amendment

Response to Arguments

10. In response to Applicants' argument that the proposed combination of Huang et al. with Bothra et al. does not appear to teach or suggest coating a substrate with a sacrificial material that fills gaps, and plasma etching to strip the sacrificial material and a hard mask substantially completely in a single plasma etch process, examiner respectfully disagree. Applicants are directed to page 2, 2nd paragraph, presented in this Office Action where the newly discovered reference Cheng et al. (U.S. Patent 6,159,821) discloses a method of stripping a hard mask from a substrate comprising an insulating material (FIG. 2: 12) (col. 2, lines 34-36) exposed within gaps (FIG. 2: 16) (col. 2, lines 33-44) patterned through the hard mask (FIG. 2: 14), comprising (col. 2, line 33 to col. 3, line 51 and FIGS. 1-11): coating the substrate (FIG. 2: 10) with a sacrificial material (FIGS. 3-4: 17) that fills the gaps (col. 2, lines 45-48); and plasma etching (col. 2, lines 54-64) to strip the sacrificial material and the hard mask "substantially" completely in a single plasma etch process (FIGS. 4-5). For this reason, examiner considers the rejection proper.

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Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D Nguyen whose telephone number is (571) 272-1865. The examiner can normally be reached on Monday-Friday (8:00 AM - 5:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (571) 272-1855. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3432 for regular communications and (703) 305-3432 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

K.N.
February 20, 2004


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